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OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

W)	AR	H. Koga et al., "Two-Dimensional Borderless Contact Pad Technology for a 0.135 μ m ² 4-Gigabit DRAM Cell," ©1997 IEEE, pp. 2.1.1-2.1.3			
	BR	Y. Mitani et al., "Buried Source and Drain (BSD) Structure for Ultra-shallow Junction Using Selective Deposition of Highly Soped Amorphous Silicon," 1996 Symposium on VLSI Technology Digest of Technical Papers, ©1996 IEEE, pp. 176-177.			
	CR	C. Mazuré et al., "Facet Engineered Elevated Source/Drain by Selective Si Epitaxy for 0.35 Micron Mosfets," IEDM 92-853, ©1992 IEEE, pp. 33.7.1-33.7.4.			
	DR	J. Sun et al., "Impact of Epi Facets on Deep Submicron Elevated Source/Drain MOSFET Characteristics," IEEE Transactions on Electron Devices, Vol. 45, No 6, June 1998, ©1998 IEEE, pp. 1377-1380.			
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	FR	J. Lee et al., "Strained Growth Behavior of Selective Silicon Epitaxy in Confined Structures," Journal of Korean Physical Society, Vol. 33, Nov. 1998, pp. S302-S304.			
	GR	T. Ohguro et al., "0.15- m Buried-Channel p-MOFSET's with Ultrathin Boron-Doped Epitaxial Si Layer," IEEE Transactions on Electron Devices, Vol. 45, No. 3, March 1998, pp. 717-721.			
	HR	T. Ohguro et al., "Undoped Epitaxial Si Channel n-MOFSET Grown by UHV-CVD with Preheating," IEEE Transactions on Electron Devices, Vol. 45, No. 3, March 1998, pp. 710-716.			
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	LR	S. Yamakawa, et al., "Drivability Improvement on Deep-Submicron MOSFET's by Elevation of Source/Drain Regions," IEEE Electron Device Letters, Vol. 20, No. 7, July 1999, pp. 366-368.			
	MR	A. Asenov et al., "Supression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1- μ m MOSFET's with Epitaxial and δ -Doped Channels," IEEE Transactions on Electron Devices Vol. 46, No. 8, August 1999, pp. 1718-1724			
	NR	H. Hada et al., "A Self-Aligned Contact Technology Using Anisotropical Selective Epitaxial Silicon for Giga-Bit DRAMs," IEDM-95-665, ©1995 IEEE, pp. 27.4.1-27.4.4			
	OR	H. Koga, et al., "A 0.23 μ m ² Double Self-Aligned Contact Cell for Gigabit DRAMs With a Ge-Added Vertical Epitaxial Si Pad," IEDM 96-589, ©1996 IEEE, pp. 22.1.1-22.1.4			
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	QR	T. Tanaka et al., "Channel Engineering Using B ₁₀ H ₁₄ Ion Implantation for Low V _{th} and High SCE Immunity of Buried-Channel PMOSFETs in 4-Gbit DRAMS and Beyond," ©1998 IEEE, 2 pages			
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